CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a primary surface of bulk material; and

a second surface of said bulk material substantially parallel to said primary surface, said second surface disposed to receive a fractional negative voltage.

2. The semiconductor device of Claim 1 further comprising a coupling for conducting said fractional negative voltage to said second surface.

3. The semiconductor device of Claim 1 wherein said fractional negative voltage is coupled to said second surface.

4. The semiconductor device of Claim 1 further comprising a voltage source to supply said fractional negative voltage.

5. The semiconductor device of Claim 1 wherein said bulk material is silicon.

6. The semiconductor device of Claim 5 wherein said silicon comprises a plurality of layers which constitute an integrated circuit.

7. The semiconductor device of Claim 1 wherein said fractional negative voltage is less than about 50 millivolts in magnitude.

8. A method of operating a semiconductor device comprising:

applying an operating voltage to said semiconductor device; and

applying a fractional negative voltage to a second surface of said semiconductor device.

9. The method of Claim 8 wherein said fractional negative voltage is applied by a wafer test machine.

10. The method of Claim 8 wherein said fractional negative voltage is applied to said semiconductor device within a semiconductor package.

11. The method of Claim 8 wherein said fractional negative voltage is produced by said semiconductor device.

12. The method of Claim 8 wherein said fractional negative voltage is less than about 50 millivolts in magnitude.

13. A semiconductor device comprising bulk material wherein said bulk material is coupled to a fractional negative voltage.

14. The semiconductor device of Claim 13 further comprising circuitry to generate said fractional negative voltage.

15. The semiconductor device of Claim 13 wherein said fractional negative voltage is generated external to said semiconductor device.

16. The semiconductor device of Claim 13 wherein said fractional negative voltage is coupled to a secondary surface of said semiconductor device.

17. The semiconductor device of Claim 16 wherein said coupling comprises a semiconductor package.

18. The semiconductor device of Claim 13 wherein said bulk material is silicon, and said silicon comprises a plurality of layers which constitute an integrated circuit.

19. A device comprising:

a primary surface of a substrate comprising an integrated circuit; and

a second surface of said substrate substantially opposed to said primary surface, said second surface disposed to receive a fractional negative voltage.

20. The device of Claim 19 further comprising a coupling for conducting said fractional negative voltage to said second surface.

21. The device of Claim 19 wherein said fractional negative voltage is coupled to said second surface.

22. The device of Claim 19 further comprising a voltage source to supply said fractional negative voltage.

23. The device of Claim 19 wherein said fractional negative voltage is less than about 50 millivolts in magnitude.

24. A device comprising:

a primary surface of a substrate comprising an integrated circuit, wherein said primary surface is disposed to receive a negative operating voltage for said integrated circuit; and

a second surface of said substrate substantially opposed to said primary surface, said second surface disposed to receive a fractional positive voltage.

25. The device of Claim 24 further comprising a coupling for conducting said fractional positive voltage to said second surface.

26. The device of Claim 24 wherein said fractional positive voltage is coupled to said second surface.

27. The device of Claim 24 further comprising a voltage source to supply said fractional positive voltage.

28. The device of Claim 24 wherein said fractional positive voltage is less than about 50 millivolts in magnitude.

29. A method comprising:

supplying a positive voltage to a top surface of a semiconductor wafer;

testing said semiconductor wafer;

responsive to a failure of said testing, applying a fractional negative voltage to a bottom side of a substrate of said wafer; and

retesting said semiconductor wafer with said negative voltage applied to said bottom side.

30. The method of Claim 29 further comprising marking said wafer with a first pass indicator in response to passing said testing.

31. The method of Claim 29 further comprising marking said wafer with a second pass indicator in response to passing said retesting.

32. The method of Claim 30 and further comprising binning said wafer based on said first pass indicator.

33. The method of Claim 29 further comprising testing said wafer at least a third time responsive to a failure of said retesting.

34. The method of Claim 29 further comprising rejecting said wafer as defective responsive to a failure of said retesting.

35. The method of Claim 29 further comprising repeating said testing, applying and retesting for a plurality of wafers.